**5. Modulus n Counter**

**AIM:** To design and implement mod - 10, mod – 7, mod - 99 asynchronous BCD counter using IC 7490 and to design and implement up, down, mod - n Binary counter using IC 74191.

**OBJECTIVE:** To know difference between regular & truncated counter as well as binary & BCD Counter

**IC’s USED:**  IC 7490, IC 74191, basic gates.

**THEORY: Part A – IC 7490**

IC 7490 is a TTL MSI (medium scale integration) decade counter. It contains 4 master slave flip flops internally connected to provide MOD-2 i.e. divide by 2 and MOD-5 i.e. divide by 5 counters. MOD-2 and Mod-5 counters can be used independently or in cascading.

It is a 4-bit ripple type decade counter. The device consists of 4-master slave flip flops internally connected to provide a divide by two and divide by 5 sections. Each section has a separate clock i/p to initiate state changes of the counter on the high to low clock transition.

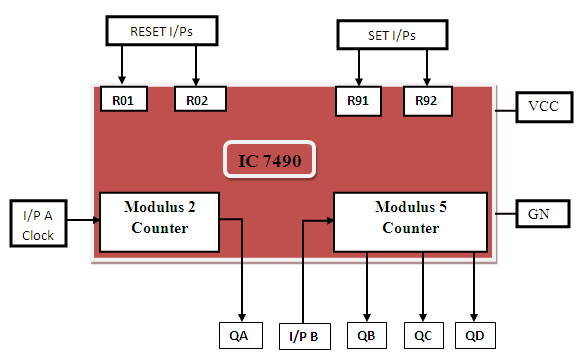
Since the o/p from the divide by 2 section is not internally connected to the succeeding stages. The device may be operated in various counting modes. In a BCD counter the CP1 input must be externally connected to QA o/p. The CP0 i/p receives the incoming count producing a BCD count sequence. It is also provided with additional gating to provide a divide by 2 counter and binary counter for which the count cycle length is divide by 5. The device may be operated in various counting modes.

There are 2 reset inputs R0(1) and R0(2) both of which need to be connected to the ‘logic 1’ for clearing all flip flops. Two set inputs Rg(1) and Rg(2) when connected to logic 1 are used for setting counter to 1001 (BCD 9).

**Pin out of IC 7490:**



**Basic internal Structure of IC 7490**:



**Function Table of MOD-2 counter:**

|  |  |  |
| --- | --- | --- |
| Input A clock | Output | Count |
|  | 0 | 0 |
|  | 1 | 1 |

**Function Table of MOD-5 counter:**

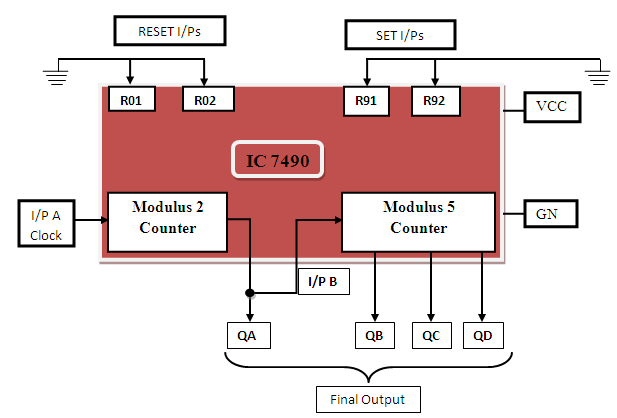
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input B clock | Output | | | Count |
| **QD** | **QC** | **QB** |
|  | **0** | **0** | **0** | **0** |
|  | **0** | **0** | **1** | **1** |
|  | **0** | **1** | **0** | **2** |
|  | **0** | **1** | **1** | **3** |
|  | **1** | **0** | **0** | **4** |

**Design of MOD-10 counter using IC 7490:**

The QA o/p the first flip flop is connected to the input B which is clock i/p of internal MOD-5 ripple counter. Due to cascading of Mod-2 and Mod-5 counters, the overall configuration the decade counters count from 0000 to 1001. After 1001 mod-5 resets to 0000 and next count after 1001 is 0000.

When QA o/p is connected to B i/p, we have the Mod-2 counter followed by Mod-5 counter. The count sequence obtained is shown in the table. It may be noted that QA changes from 0 to 1 the state of Mod-5 counter doesn’t change, whereas when QA changes from 1 to 0 the Mod-5 counter goes to the next state.

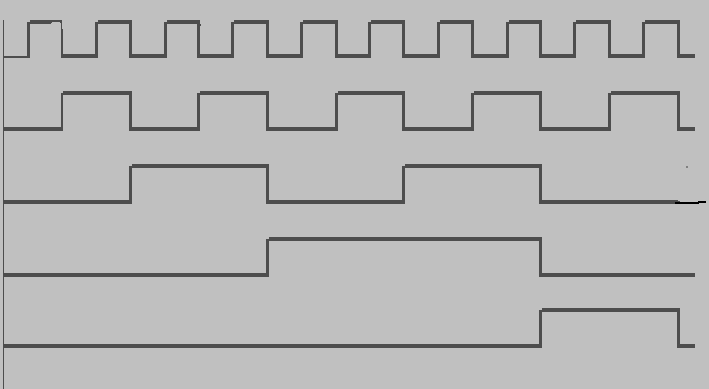
**Logic Diagram MOD-10 counter using IC 7490:**

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**Function table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| I/p clock | Output | | | | Count |
| **QD** | **QC** | **QB** | **QA** |
|  | **0** | **0** | **0** | **0** | **0** |
|  | **0** | **0** | **0** | **1** | **1** |
|  | **0** | **0** | **1** | **0** | **2** |
|  | **0** | **0** | **1** | **1** | **3** |
|  | **0** | **1** | **0** | **0** | **4** |
|  | **0** | **1** | **0** | **1** | **5** |
|  | **0** | **1** | **1** | **0** | **6** |
|  | **0** | **1** | **1** | **1** | **7** |
|  | **1** | **0** | **0** | **0** | **8** |
|  | **1** | **0** | **0** | **1** | **9** |

**Timing diagram of mod10:**

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0

0

0

0

0

0

0

0

1

1

1

0

0

0

0

1

1

1

0

0

1

1

1

0

1

0

1

1

0

0

0

1

1

0

0

0

0

0

0

0

1

0

0

0

QB

QC

QD

QA

CLK

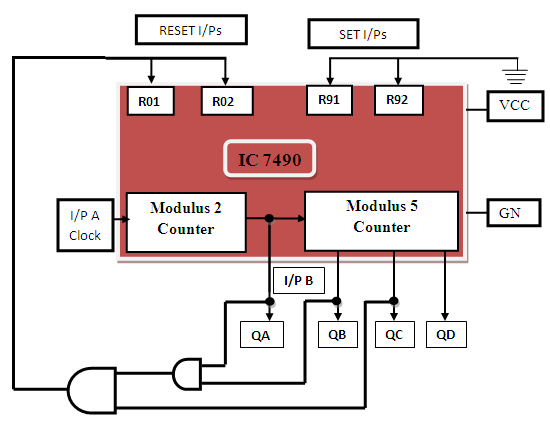
**Design of Mod-7 Counter using IC 7490:**

Mod-7 counter counts through seven states from 0 to 6 counters and it should reset as soon as the count becomes 7. The o/p of reset logic should be 1 corresponding to invalid states. The reset logic o/p should be applied to pin 2 and 3.

**Truth Table of Reset Logic:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **QD** | **QC** | **QB** | **QA** | **Y** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |

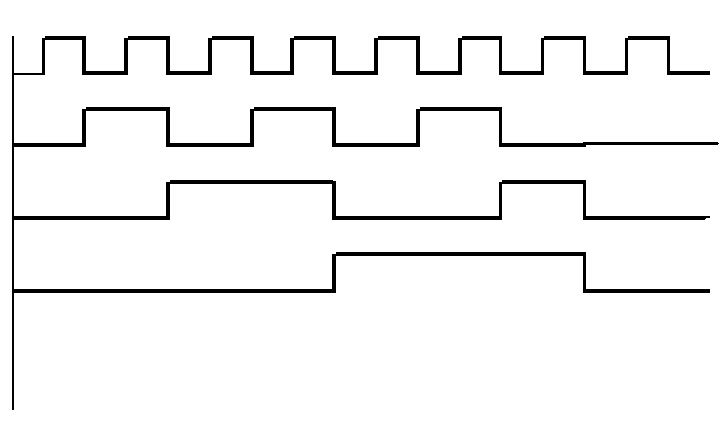
**Logic Diagram Mod 7 Counter using IC 7490 :**

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**Function table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| I/p clock | Output | | | | Count |
| **QD** | **QC** | **QB** | **QA** |
|  | **0** | **0** | **0** | **0** | **0** |
|  | **0** | **0** | **0** | **1** | **1** |
|  | **0** | **0** | **1** | **0** | **2** |
|  | **0** | **0** | **1** | **1** | **3** |
|  | **0** | **1** | **0** | **0** | **4** |
|  | **0** | **1** | **0** | **1** | **5** |
|  | **0** | **1** | **1** | **0** | **6** |

**Timing diagram of mod7:**

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CLK

0

0

1

1

0

0

1

0

1

1

0

0

0

1

1

0

1

0

0

0

1

0

0

0

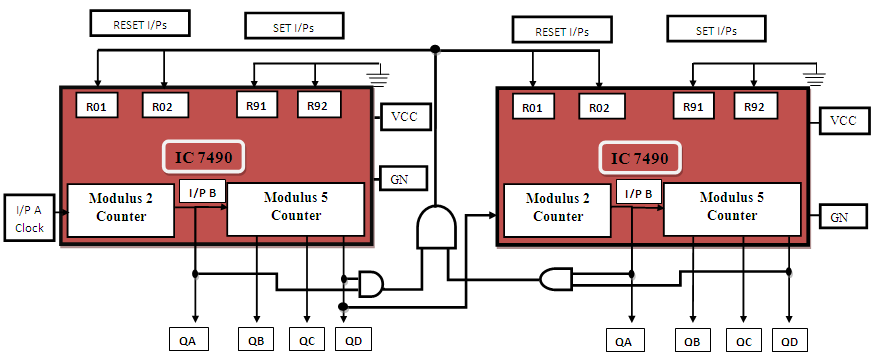
QCA

QBA

QAA

**Design of Mod-99 using IC 7490:**

For Mod-99 two IC 7490’s will be required. Hence to implement a divide by 99 counter we have to use two decade counters IC’s. A divide by 99 counter counts 99 states from 0 to 98 and the counter should reset as soon as the count becomes 99. So in order to reset the counter of 99 connect the Q o/p which are equal to 1 in the count of 99 to an ‘And’ gate & then connect and o/p to the reset i/p of both IC’s.

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**Design of MOD 16 counter using IC 7490:**

**B) IC 74191 – Theory**

IC74191 is 4-bit binary synchronous, reversible, up down counter. It contains 4 master slave flip flops with internal gating and steering logic to provide asynchronous reset and synchronous count up/down operations, its asynchronous parallel capability permits the counter to be preset to any desire number D0 to D3 are the parallel data inputs. Information present on the parallel data inputs D0 to D3 is loaded into the counter and appears on the output when the load PLinput is low.Thisoperation overrides the counting function .Counting is inhabited by the high level on the enable G input, when G input is low internal state changes are initiated synchronously by the low to high transitions of the clock inputs the up/down input signal determines the direction of input.

**Function Table :**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Operating mode** | **Inputs** | | | | | **Outputs** |
| **PL** | **U/D** | **G** | **CLK** | **Dn** |  |
| Parallel load | L | X | X | X | L | L |
|  | L | X | X | X | H | H |
| Count up | H | L | 0 | ↑ | X | Count up |
| Count down | H | H | 0 | ↑ | X | Count down |
| Hold(No change) | H | X | H | X | X | No change |

**Pin details –**

D0 to D3 input lines, PL parallel load

G is Enable input – enabling the counting.

Q0 to Q3 output lines.

Down/up determines the direction of counting.

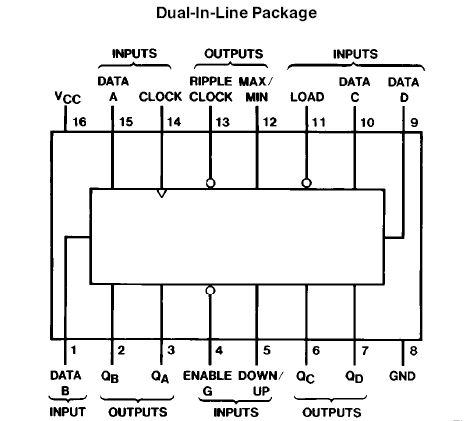
Clk clock input for counter.

Terminal Count : Max(1111) min(0000). For these states signal goes high for 1clock

pulse.

Ripple clock: Clock input for next higher state.

**Pin Diagram :**



**Up counter- Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clk Pulses** | **QA** | **QB** | **QC** | **QD** |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |

**Logic Diagram**

Clock D3 D2 D1 D0 PL

14 9 10 1 15 11

IC 74191

G RC

U / D MAX / MIN

UP/Down 5 13 RC

G 4 7 6 2 3 12 Q3 Q2 Q1 Q0 TC

NC

NC

NC

Outputs

no connection

**Steps-**

* Connect the circuit as shown above.
* Apply clock i/p to pin no.14
* Connect U/D to GND.
* Verify the output according to truth table.

**Down counter- Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK Pulses** | **Q3** | **Q2** | **Q1** | **Q0** |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |
| 2 | 1 | 1 | 0 | 1 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 1 | 0 | 1 | 1 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 1 | 0 | 0 | 1 |
| 7 | 0 | 0 | 0 | 0 |
| 8 | 0 | 1 | 1 | 1 |
| 9 | 0 | 1 | 1 | 0 |
| 10 | 0 | 1 | 0 | 1 |
| 11 | 0 | 1 | 0 | 0 |
| 12 | 0 | 0 | 1 | 1 |
| 13 | 0 | 0 | 1 | 0 |
| 14 | 0 | 0 | 0 | 1 |
| 15 | 0 | 0 | 0 | 0 |

U/D D3 D2 D1 D0 PL

Clk

Clock  **IC 74191**

G RC

MAX / MIN

G Q3 Q2 Q1 Q0 TC

vcc

NC

NC

Outputs

no connection

vcc

**Logic diagram of down counter**

**Steps-**

* Connect the circuit as shown above.
* Apply clock i/p to pin no.14
* Connect U/D to VCC.
* Verify the output according to truth table.

With the help of IC74191 we can implement **truncated up/down counter** by using following logic –

* Connect data input line to particular count you want to load
* According to requirement make Truth table
* Draw the K-map
* Find out Boolean expression
* Draw the logic diagram and that is the combinational logic for your count and apply the output of that circuit to PL
* According to requirement we get the UP and down counting

**Presettable up/down counter**

Combinational Circuit

CLOCK D3 D2 D1 D0

TC

U / D **74191**  RC

G PL

Up/down Q3 Q2 Q1 Q0 PL

Q3 Q2 Q1 Q0

Preset Count

**Mod 11 counter**

Implementation of presetttable mod up/down counter using IC- 74LS191

1. Load Data on data lines D0 to D3 (0101).
2. Counter will go through the states from 0101 ,0110,…1111 in up counter and 0101 to 0000 in down counter.
3. The logic circuit should be designed in such a way that only when all the outputs are high, output of the reset circuit should be low and the counter should jump to state 5. It should again start counting from 0101 to 0000,

**State Table**

**Down Counter UP Counter**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Counter state / Clock pulse** | **Q3** | **Q2** | **Q1** | **Q0** |
| 1 | 0 | 1 | 0 | 1 |
| 2 | 0 | 1 | 1 | 0 |
| 3 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 0 | 1 |
| 6 | 1 | 0 | 1 | 0 |
| 7 | 1 | 0 | 1 | 1 |
| 8 | 1 | 1 | 0 | 0 |
| 9 | 1 | 1 | 0 | 1 |
| 10 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Counter state /**  **Clock pulse** | **F/F outputs** | | | |
| **Q3** | **Q2** | **Q1** | **Q0** |
| 1 | 0 | 1 | 0 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 0 | 0 | 0 | 1 |
| 6 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 0 | 1 |

IC 74191 is 4 bit counter. Thus it counts 0000 to 1111 different 16 states. For MOD11 counter we require different 11 states so 5 steps must be skipped from 16 states. We get MOD11 by presetting counter to value 5 .

GND

vcc

GND

GND

vcc

Clk 16 A B C D

RC

U / D MAX / MIN

G QA QB QC QD

13

12

5 Q3 Q2 Q1 Q0 11

14 8 7 6 2 3

11

32

32

32

**N**C

**High or Low**

**Conclusion:**

**FAQs:**

1. What do you mean modulus counter?

It represents the number of possible states of counter.

2. How will you use the 7490 IC to design symmetrical divide by 10 frequency counter?

The divide by 5 circuit followed by divide by 2 circuit will give symmetrical output.

1. Where counters are used? Give real life example of counter.

Binary counter – An N stage counter that recycles after 2 Ncount. The count proceds in specified binary sequence.

5. Counter, Presetable- A counter which can be set to a desired value before the start of the counting/

6. UP/Down counter – A counter that can count in both up and down direction depending upon a control input.